IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 2, Issue 3, June-July, 2014
ISSN: 2320 – 8791 (Impact Factor: 1.479)
www.ijreat.org

Optimal Built-In Self Repair Analyzer for Word-Oriented Memories

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***Abstract*—This paper presentsoptimalbuilt-in self-repair analyzer using built in self repair tests with BSLFSR and PBCAM. According to this optimal built in self repair is advanced than existing methods because it is used for byte oriented memories and having error detection and correction methods. The proposed methods using the BSLFSRto reduce both the transition and the power consumption & PBCAM to reduce the searching time in MRA. The Must Repair Analyser enables the fault bits to do the error correction using spare wires.It requires only a single test, even in the worst case andsupports various types of word-oriented memories.**

***Index Terms*—Built-in self repair test (BIST), memory test, redundancy allocation, repair analysis, spare allocation.**

I. INTRODUCTION

The design flow for a SOC aims to develop this hardware and software in parallel. Therefore, the overall SOC yield is dominated by the memory yield, and optimizing the memory yield plays a crucial role in the SOC environment. To improve the yield, memory arrays are usually equipped with spare elements, and external testers have been used to test the memory arrays and configure the spare elements. On the other hand, the SOC environment, combined with shrinking technology, allows us more area for on-chip test infrastructure at lower cost than before, which makes feasible a variety of built-in self test (BIST) and built-in self-repair (BISR) techniques for reducing the test time, and also it is to test the memory arrays.

A circuit is tested once and for all, with the hope that once the circuit is verified to be fault free it would not fail during its expected life-time, it is called off-line testing. However, this assumption does not hold for modern day ICs, based on deep sub-micron technology, may develop failures even during operation within expected life time. To cater to this problem sometimes redundant circuitry are kept on-chip which replace the faulty parts.

To enable replacement of faulty circuitry, the ICs are tested before each time they startup. If a fault is found, a part of the circuit (having the fault) is replaced with a corresponding redundant circuit part (by re-adjusting connections). Testing a circuit every time before they startup, is called Built-In-Self-Test (BIST). Once BIST finds a fault, the readjustment in connections to replace the faulty part with a fault free one is a design problem.

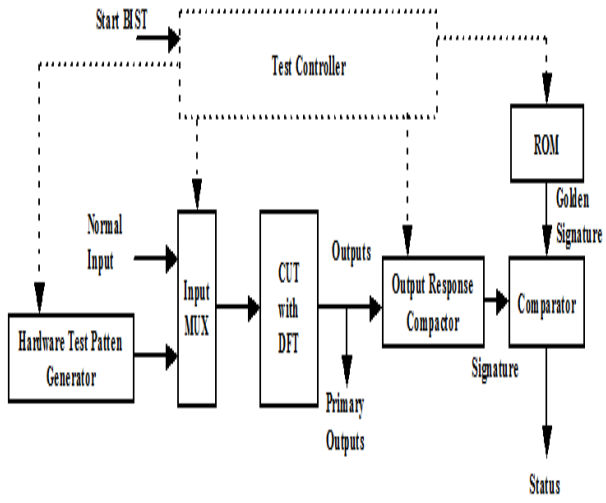

Fig.1. Basic Architecture of BIST

In accordance with this trend, built-in redundancy allocation (BIRA) approaches have been proposed as part of BISR. The BISRA use parallel sub-analyzers, each of which evaluates a solution candidate. It has the sub-analyzers for all solution candidates, provides the optimal repair rate with a single test. The sub-

analyzer consists of content addressable memory (CAM) of row with r entries (r is the number of repair rows) and a column CAM with c entries (c is the number ofrepair columns), and $\binom{r+c}{c}$sub-analyzers. So, to reduce size in memories with many spare elements, subsequent studies have been analyzed with required algorithms needed and applied to design.

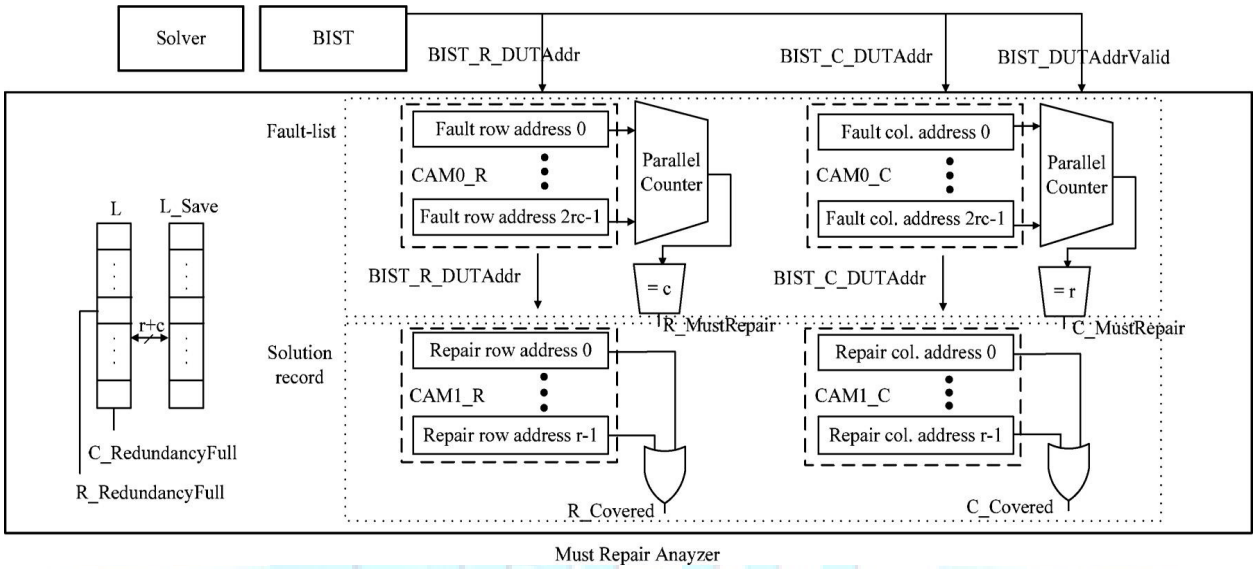

Fig.2. Proposed on-chip infrastructure and must repair analyzer details.

We propose a combinational circuit, which can be designed in various ways to meet the requirements for area and test time. For fast output generation, it can generate the next solution candidate in a single duty cycle.

II.MUST REPAIR ANALYZER

The Must Repair Analyzer (MRA) circuit diagram is as shown in Fig 2. It consists of a pair of CAMs for fault addresses, called the fault-list, and a pair of CAMs for a repair solution, called the solution record. The memory is repaired during testing by storing faulty addresses in registers. These addresses can be streamed out after test completion. Furthermore, the application started immediately after the memory BIST passes. In the fault-list, each CAM has one extra valid bit for each word, and the valid bits are initialized to "0" in the starting. Since the CAMs assert "1" at the valid bit position for write and match operation, only written entries can be matched. During the test, if the BIST engine detects a fault, it sends the fault address to the MRA on the fly through BIST_R_DUTAddr and BIST_C_DUTAddr, continues the test. The row (column) fault address is compared against row (column) CAM entries.

The 100% normalized repair rate is called the optimal repair rate.

The number of matched entries is efficiently counted by a parallel counter. If the number of the matched entries equals in the row (column) CAM, the must-repair condition and R_MustRepair row (column) indicated by the fault address satisfies(C_MustRepair) signal is asserted. If the fault address triggers neither the row nor column must-repair condition, MRA writes the row and column address in the row and column CAMs, respectively

An efficient implementation of a word-oriented memory of type where any faulty column can be replaced with an available spare column without any restriction shown in Fig.3.

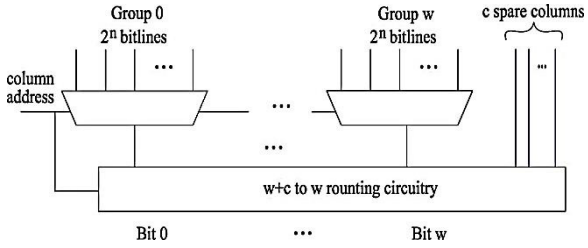

Fig.3. Column circuitry of a word-oriented memory.

III. SOLVER AND MRA OPERATIONS

We propose a Built in infrastructure forbyte-oriented memories. Our repair analyzer requires only a single test and provides the optimal repair rate. The MRA consists of a pair of CAMs for fault addresses, called the *fault-list*, and a pair of CAMs for a repair solution, called the *solution record*.

SOLVER include the address, faults on the address do not affect the final analysis any more. So, such faults do not need to be stored, and we can collect all necessary information for the final analysis during a single test. Once the must-repair analysis is done, *BIST_Done* signal is asserted and the final analysis report is started. In the final analysis, the SOLVER module controls over MRA. The operation of the SOLVER and the MRA in the final analysis phase is shown in Fig. 4.

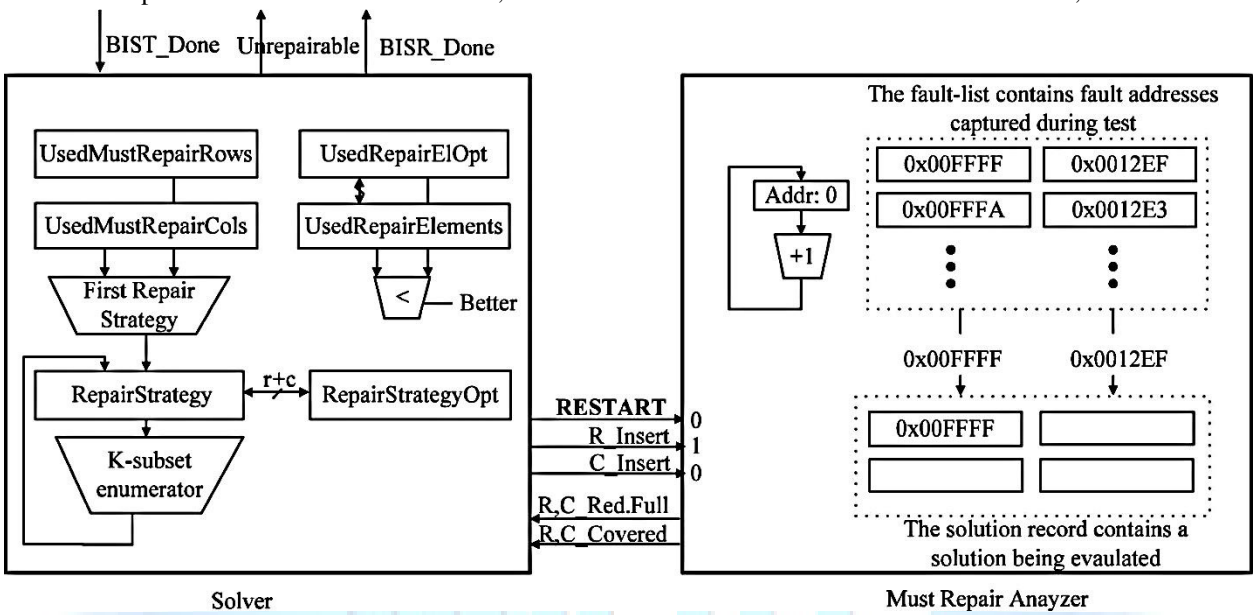

Fig.4. Solver details and MRA operation in the final analysis phase: If the fault address being read is not covered by the current solution, depending on R_Insertor C_Insert, the row or column fault address is added to the current solution.

In the repair strategy, and the SOLVER generates the next repair strategy and asserts the *RESTART* signal generated directly from the current repair strategy by a combinational circuit called *K-subset enumerator*,When the *RESTART* signal becomes 1, the MRA restores the starting state, and the next repair strategy starts being evaluated. By this way, the SOLVER produces the solution space and can find a solution there.

TABLE I
BIT REPRESENTATIONS OF REPAIR STRATEGIES

REPAIR STRATEGY	BIT REPRESENTATION
CRRC	0110
CRCR	0101
CCRR	0011
RRCC	1100
RCRC	1010
RCCR	1001

V.BIT SWAPPING LFSR

Low-transition linear feedback shifts register (LFSR) that is based on shift register observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR is composed of an LFSR and a 2 × 1 multiplexer. To generate test patterns for scan-based built-in self-tests reduces the number of transitions that occur at the scan-chain input during scan shift operation. So, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power in the test cycle or while scanning out a response to a signature analyzer.

These techniques have animproved effect on average and peak-power reductions with negligible effect on fault coverage or test application time. The BS-LFSR is used with the proposed scan-chain-ordering algorithm, the average and peak powers are reduced. The bit-swapping linear feedback shift register that is based on a simple bit swapping technique applied to the output sequence of a conventional LFSR and

designed using a conventional LFSR and a 2 × 1 multiplexer.

The BS-LFSR reduces the average and instantaneous weighted switching activity during test operation by reducing the number of transitions in the scan input of the circuit under test.

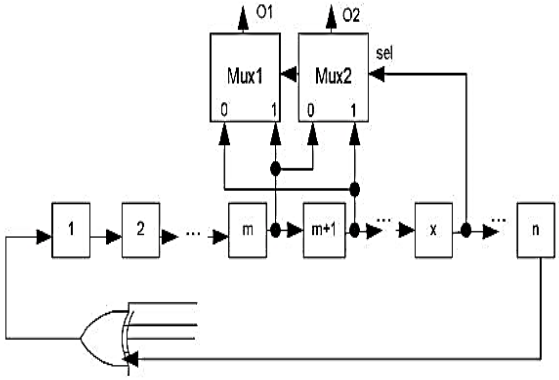

Fig.5. Bit Swapping LFSR

The BS-LFSR is improving the speed by increasing the transitions and reducing the power consumption shown in Table II.

TABLE II
COMPARISON TABLE FOR POWER CONSUMPTION

S.No	Process	Power Consumption(mw)
1.	Existing Method (LFSR)	373
2.	Proposed Method (BS-LFSR)	113

VI.PRE COMPUTATIONAL CAM

Content-addressable memory (CAM) is used in more applications,such as lookup tables, databases, associative computing, and networking,that require high-speed searches of its ability to improve applicationperformance by using parallel comparison reducing search time.Even though the use of parallel comparison results in reduced search time. Italso significantly increases power consumption. We proposea Block-XOR approach for improving the efficiency of low power precomputationbased CAM (PB-CAM). By mathematical analysis PBCAM effectively reduce the number of comparison operationsby half.

Comparedwith the ones-count PB-CAM system, the experimental results showthat our proposed Block-XOR Pre computational CAM system can achieve greater power reductionwithout the need for a special CAM cell design shown in Table III. This implies thatour approach is more flexible and adaptive for general designs.

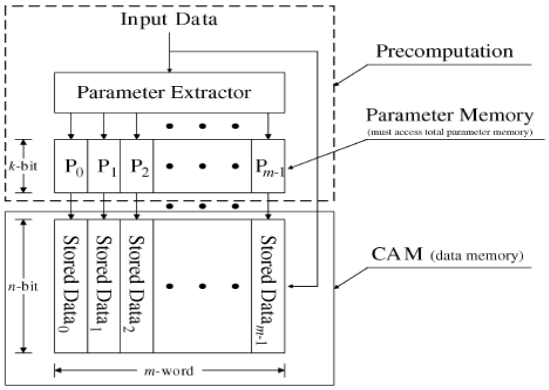

Fig.6.Memory organization of the Pre computational based CAM architecture (PB-CAM)

TABLE III
COMPARISON TABLE FOR TIME DELAY

S.No	Process	Time Delay (ns)
1.	Existing Method (CAM)	8.313
2.	Proposed Method (PB-CAM)	2.872

We have implemented the infrastructure in 130-nm technology for a memory array with four repair rows and four repair columns, and the operating frequency is 400 MHz and 600 cycles in memory array with experimental results in VII.

VII.EXPERIMENTAL RESULTS

The final simulation analysis performed with minor modifications is that given multiple faults within a

word andpossible ways to fix them; a repair row is used, or all faults are fixed by a repair column.

Thus the fault bit in the word oriented memories are spotted and removed with reduced power consumption and time using BS-LFSR and PB-CAM respectively using the VHDL codings shown in Fig 7 and Fig 8 by Modelsim simulated output.

Also, the power consumption and Time delay results are verified using Xilinx software.

A. ERROR SPOTTING

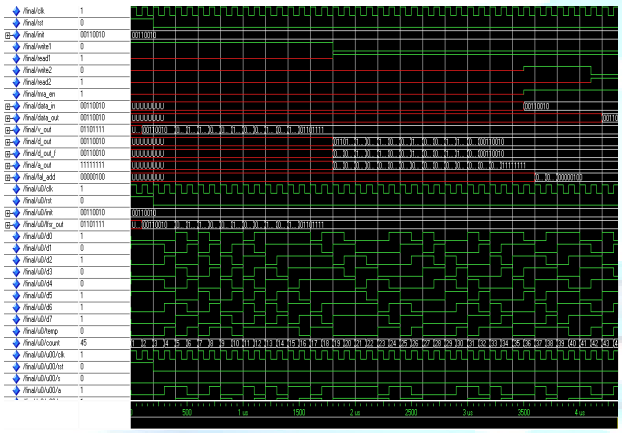

Fig.7. Error Spotting

Spotted errors are removed using Solver circuit.

B. ERROR REMOVING

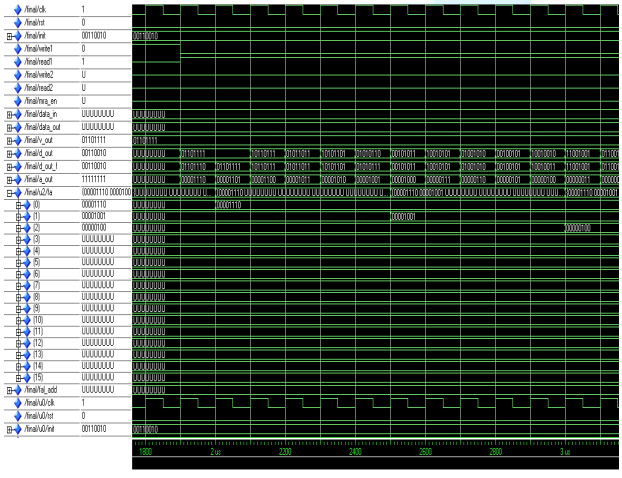

Fig.8.ErrorRemoving

VIII.CONCLUSION

We have proposed aBuilt in infrastructure for repair analysis with the optimal repair rate for byte word oriented memories meet area, power and test time requirements. The optimal built in self repair analyzer used to spot and remove the errors in byte oriented memories with in a single test. The proposed methods using the BSLFSR to reduce both the transition and the power consumption to 113mW. This is achieved by using low-cost on-chip selection mechanisms, which are instrumental in very accurate and power reduction identification of failing rows andcolumns. The proposed methods using PBCAM is to search the fault addressesimmediately using precomputational circuits in MRA to reduce the searching time to 2.872ns.

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